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FORM PTO-1449

(Rev. 2-32)

U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT
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ATTY. DOCKET NO.: P-9201.02	SERIAL NO: 10/067,570
APPLICANT: Schu et al.	
FILING DATE: February 5, 2002	GROUP:

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE ISSUED	INVENTOR NAME	U.S. CLASS	U.S. SUB-CLASS	FILING DATE IF APPROPRIATE
~	AA	5,986,466	11/16/99	Sobelman et al	326	39	
|	AB	5,822,609	10/13/98	Richter	395	800.35	
|	AC	5,752,070	05/12/98	Martin et al.	395	800	
|	AD	5,655,090	08/05/97	Weingart	395	800.25	
|	AE	5,305,463	04/19/94	Fant et al.	395	800	
|	AF	5,186,169	02/16/93	Schaldach	128	419 PG	
|	AG	5,014,057	05/07/91	Mintzer	341	161	
|	AH	4,515,159	05/07/85	McDonald et al.	128	419 PG	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE PUBLIC-ATION	COUNTRY	INT. CLASS	INT. SUB-CLASS	TRANSLATION YES	TRANSLATION NO
~	AH	EP 0 911 061 A2	28.04.99	EP	A61N	1/36		
|	AI	GB 2 335 293 A	15.09.99	UK	G06F	1/32		
|	AJ	GB 2 330 673 A	28.04.99	UK	G06F	9/22 9/38		

OTHER DOCUMENTS (Including Author, Title, Date Pertinent Pages, Etc.)

NO DATE ~			"Clockless Logic Overview," @ http://www.sanders.com/hpe/CL/Overview.html
~			Cogency Technology, @ http//:www.cogency.co.uk/tech/index.html, © 1999, 8 p.
			Fant et al., "NULL Convention Logic™," Theseus Logic, Inc., 1997, 35 p.
			Jacobs et al., "A Fully Asynchronous Digital Signal Processor Using Self-Timed Circuits," IEEE Journal of Solid-State Circuits, vol. 25, no. 6, p. 1526-1537 (December 1990)
|			Wang et al., "Technology Independent Design Using NULL Convention Logic™," Theseus Logic, Inc., 10/19/98, 19 p.

EXAMINER ~	DATE CONSIDERED 9/24/4

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.